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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2006

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 500.00

Complete if Known	
Application Number	09/752,874
Filing Date	December 29, 2000
First Named Inventor	Lily P. LOOI
Examiner Name	N. Patel
Art Unit	2112
Attorney Docket No.	P9869

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☑ Deposit Account Deposit Account Number: 05-0221 Deposit Account Name: Intel Corporation

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☑ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, except for the filing fee

☑ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☑ Credit any overpayments

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES Fee ($)	FILING FEES Small Entity Fee ($)	SEARCH FEES Fee ($)	SEARCH FEES Small Entity Fee ($)	EXAMINATION FEES Fee ($)	EXAMINATION FEES Small Entity Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 20 or HP =	_____	x _____	= _____

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 3 or HP =	_____	x _____	= _____

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims Fee ($)	Fee Paid ($)
_____	_____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
_____ - 100 =	_____ / 50 =	_____ (round up to a whole number)	x _____	= _____

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other (e.g., late filing surcharge): Appeal Brief Fee	500.00

SUBMITTED BY

Signature	/Paul E. Steiner/	Registration No. (Attorney/Agent) 41,326	Telephone 703-633-6830
Name (Print/Type)	Paul E. Steiner		Date November 20, 2006

Intel Corporation
4040 Lafayette Center Drive
Chantilly, VA 20151

FAX

Urgent and Confidential

Date: November 20, 2006

TO:	**USPTO**	
	Examiner	N. Patel
	Art Unit	2112
	Fax Number	571-273-8300
FROM:	**Paul E. Steiner**	
	Fax Number	703-633-0933
	Phone Number	703-633-6830
SUBJECT:	Application Number	09/752,874
	Inventor(s)	Lily P. LOOI, et al.
	Date Filed	December 29, 2000
	Docket Number	P9869
	Title	APPARATUS AND METHOD FOR INTERRUPT DELIVERY

INCLUDED IN THIS TRANSMISSION:

Fax Cover Sheet	1 page
Fee Transmittal	1 page
Transmittal	1 page
Appeal Brief	26 pages

I hereby certify that the above listed correspondence is being facsimile transmitted to the USPTO to: Commissioner for Patents, PO BOX 1450, Alexandria, VA 22313-1450 on November 20, 2006.

Cathy Dikes Cathy DiKes

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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission: 29

Application Number	09/752,874
Filing Date	December 29, 2000
First Named Inventor	Lily P. Looi
Art Unit	2112
Examiner Name	N. Patel
Attorney Docket Number	P9869

ENCLOSURES *(Check all that apply)*

- [✓] Fee Transmittal Form
  - [ ] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Reply to Missing Parts/ Incomplete Application
  - [ ] Reply to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
  - [ ] Landscape Table on CD
- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
- [✓] Appeal Communication to TC (Appeal Notice, Brief, Reply Brief)
- [ ] Proprietary Information
- [ ] Status Letter
- [✓] Other Enclosure(s) (please identify below):
  Fax Cover Sheet

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Intel Americas		
Signature	/Paul E. Steiner/		
Printed name	Paul E. Steiner		
Date	November 20, 2006	Reg. No.	41,326

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

Signature	Cathy Dikes		
Typed or printed name	Cathy Dikes	Date	November 20, 2006

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and1.14. This collection is estimated to 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: **Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:

Lily P. LOOI, et al.

Serial No.:	09/752,874	Group Art Unit:	2112
Filed:	December 29, 2000	Examiner:	N. Patel
FOR:	APPARATUS AND METHOD FOR INTERRUPT DELIVERY		

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant submits this appeal brief, thus perfecting the notice of appeal filed on September 18, 2006.

The required headings and subject matter follow.

(i) *Real party in interest.*

This case is assigned of record to Intel Corporation, who is the real party in interest.

(ii) *Related appeals and interferences.*

There are no known related appeals and / or interferences.

(iii) *Status of claims.*

Claims 1-26 are pending in the application. Claims 1-7 and 9-26 stand rejected. The rejections of claims 1-7 and 9-26 are being appealed.

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(iv) ***Status of amendments.***

No amendments to the claims have been filed after the final rejection. The attached Claims appendix reflects the current status of the claims.

(v) ***Summary of claimed subject matter.***

With respect to independent claim 1, some embodiments of the invention involve an interrupt delivery system, including a first pair of scaleable node controllers (e.g. SNC 22 and SNC 26, see Fig. 2 and page 5, lines 9-14), wherein each of said scaleable node controllers supports at least one microprocessor (e.g. processors 24a-d and processors 28a-d, see Fig. 2 and age 5, lines 9-14), a first scalability port switch (e.g. SPS 30, see Fig. 2 and page 5, lines 9-14) coupled to each of said scaleable node controllers, wherein said first scalability port switch is to receive an interrupt request (e.g., from IOH 32, see page 5, lines 15-21), determine an address of one of said scaleable node controllers from said interrupt request (e.g., see page 5, lines 18-25) and transmit said interrupt request to said one of said scaleable node controllers (e.g., see page 5, lines 22-23).

With respect to independent claims 9 and 18, some embodiments of the invention involve a method for delivering an interrupt request in a multi-node computer system, including receiving an interrupt request at a scalability port switch (e.g. block 64 in Fig. 5, see page 7, lines 30-31), determining an address of a scaleable node controller to receive said interrupt request (e.g. block 66 in Fig. 5, see page 8, lines 3-6), and transmitting said interrupt request to said scaleable node controller (e.g. block 66 in Fig. 5, see page 8, lines 7-8).

(vi) ***Grounds of rejection to be reviewed on appeal.***

I. Claims 1-3, 9-12, 16-21, and 25-26 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,987,538 (Tavallaei).

II. Claims 1-3, 9-12, 14-21, and 23-26 are rejected under 53 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,944,809 (Olarig).

III. Claims 4 and 5 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Tavallaei in view of U.S. Patent No. 6,119,191 (Neal).

IV. Claims 6 and 7 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Tavallaei, in view of Neal, and further in view of Intel's Multiprocessor Specification, dated May 1997 (MP).

V. Claims 13 and 22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Tavallaei in view of U.S. Patent No. 6,189,065 (Arndt).

VI. Claims 13 and 22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Olarig in view of Arndt.

(vii) ***Argument.***

I. The rejection of claims 1-3, 9-12, 16-21, and 25-26 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,987,538 (Tavallaei) is in error and should be reversed.

Claims 1-3

In order to anticipate, the reference must identically disclose each claim element. In fact, Tavallaei does not identically disclose many of the recited claim elements when properly construed.

THE EXAMINER MISCONSTRUES THE CLAIM TERM 'SCALEABLE NODE CONTROLLER.'

The office action asserts that component 14 in Figure 2 of Tavallaei corresponds to the recited scaleable node controllers. However, Tavallaei describes component 14 as a local advanced programmable interrupt controller (APIC). A local APIC is not identical to a scaleable node controller.

The Examiner does not answer and apparently concedes applicants' argument that the different terminology in fact describes different structure and functionality. The Examiner does not answer and apparently concedes applicants' argument that every 'controller' does not perform the same function as every other 'controller'. The Examiner does not answer and apparently concedes applicants' argument that one skilled in the art would appreciate that a node controller performs a different function than an interrupt controller. The Examiner does not answer and apparently concedes applicants' argument that one skilled in the art would appreciate that a node controller has a different structure from an interrupt controller. The Examiner does not answer and apparently concedes applicants' argument that a node controller may have suitable structure to participate in an interrupt handling scheme, but an

interrupt controller would not have suitable structure to perform the function of controlling a node of a multi-node system.

Applicants respectfully requested that the Examiner provide a reasoned response to the foregoing arguments in order to reduce issues for appeal, noting that applicants consider each unanswered argument as conceded for the purposes of appeal. The only response to the foregoing arguments that applicants can identify is the single new paragraph occurring in the office action, which is reproduced below:

> **53. In response to applicant's argument that since the terminology used in the references is different from the claim language, the reference do not read on the claims. However, there is no clear definition of any of the components claimed. Therefore, examiner has broadly and reasonably interpreted the claim language.**

Applicants do not, as asserted by the Examiner, argue simply that because the terminology is different the reference does not read on the claims. The Examiner can refer back three paragraphs to review applicants' concrete, technical arguments as to why the different terminology actually refers to important differences in the technology.

The question is not whether applicants' specification provides a discrete definition for each claim recitation. Applicants submit that providing such discrete definitions in a patent application is the exception, rather than the norm. When performing claim construction, the Examiner may consult the specification for such definitions, but in their absence the claim term must be construed as it would be understood by one of ordinary skill in the art as of the filing date of the application. Does the Examiner seriously contend that as of the filing date of the present application, a node controller would have no clear meaning to one of ordinary skill in the art?

The Examiner commits clear legal error in his claim construction. As is set forth in MPEP § 2111.01(II), "[T]he ordinary and customary meaning of a claim term is the

meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, *i.e.*, as of the effective filing date of the patent application." Several examples set forth in MPEP § 2111.01(II) specifically state that where no definition is provided in the specification, the claim terms should be interpreted with the ordinary and customary meaning the terms would have to one skilled in the art. The Examiner has not even attempted to identify or set forth what the term 'scaleable node controller' would mean to a person of ordinary skill in the art at the time of the invention. This is clear legal error which requires reversal of the rejection.

The Examiner uses the fact that the specification does not provide a definition for these terms as an excuse to substitute his own, unreasonably broad definition of the terms. In the Examiner's view, any component that performs any control function in connection with any processing element reads on a scaleable node controller. Applicants submit that this may be the broadest possible interpretation, but it is not a reasonable interpretation and is also legally erroneous by failing to consider what the disputed terms would mean to one skilled in the art.

The Board can resolve this error by answering the following simple question. Namely, would one of ordinary skill in the art as of December 29, 2000 (the filing date of the present application), without any knowledge of applicants' own invention, have considered the APIC 14 described by Tavallaei to be a scaleable node controller? Applicants' submit that the answer to this question is no, and the rejection should be reversed.

THE EXAMINER MISCONSTRUES THE CLAIM TERM 'SCALABILITY PORT SWITCH.'

The office action asserts that component 26 in Figure 2 of Tavallaei corresponds to the recited scalability port switch. However, Tavallaei describes component 26 as an external input / output advanced programmable interrupt controller (I/O APIC). An I/O APIC is not identical to a scalability port switch.

As previously pointed out, the Examiner does not answer and apparently concedes applicants' argument that the different terminology in fact describes different structure and functionality. The Examiner does not answer and apparently concedes applicants' argument that every 'I/O' controller does not perform the same function as every other I/O switch. The Examiner does not answer and apparently concedes applicants' argument that one skilled in the art would appreciate that a port switch performs a different function than an I/O interrupt controller. The Examiner does not answer and apparently concedes applicants' argument that one skilled in the art would appreciate that a port switch has a different structure from an I/O interrupt controller. The Examiner does not answer and apparently concedes applicants' argument that a port switch may have suitable structure to participate in an interrupt handling scheme, but an I/O interrupt controller would not have suitable structure to perform the function of switching ports of a multi-node system. The Examiner does not answer and apparently concedes applicants' argument that in some applications a port switch may include structure to resolve node addresses and that the I/O APIC 26 appears to lack such structure.

In applicants' prior response, applicants respectfully requested that the Examiner provide a reasoned response to the foregoing arguments in order to reduce issues for appeal. Applicants consider each unanswered argument as conceded for the purposes of appeal. The Examiner has declined to do so.

Applicant again notes that when performing claim construction, the Examiner may consult the specification for discrete definitions of claim terms, but in their absence the claim term must be construed as it would be understood by one of ordinary skill in the art as of the filing date of the application. Does the Examiner seriously contend that as of the filing date of the present application, a port switch would have no clear meaning to one of ordinary skill in the art?

The Examiner again commits clear legal error in his claim construction. As is set forth in MPEP § 2111.01(II), "[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at

the time of the invention, *i.e.*, as of the effective filing date of the patent application." Several examples set forth in MPEP § 2111.01(II) specifically state that where no definition is provided in the specification, the claim terms should be interpreted with the ordinary and customary meaning the terms would have to one skilled in the art. The Examiner has not even attempted to identify or set forth what the term 'scalability port switch' would mean to a person of ordinary skill in the art at the time of the invention. This is clear legal error which requires reversal of the rejection.

The Examiner uses the fact that the specification does not provide a definition for these terms as an excuse to substitute his own, unreasonably broad definition of the terms. In the Examiner's view any component that performs an I/O function reads on a scalability port switch. Applicants submit that this may be the broadest possible interpretation, but it is not a reasonable interpretation and is also legally erroneous by failing to consider what the disputed terms would mean to one skilled in the art.

The Board can resolve this error by answering the following simple question. Namely, would one of ordinary skill in the art as of December 29, 2000 (the filing date of the present application), without any knowledge of applicants' own invention, have considered the I/O APIC 26 described by Tavallaei to be a scalability port switch? Applicants' submit that the answer to this question is no, and the rejection should be reversed.

THE EXAMINER'S THEORY OF INHERENCY IS LEGALLY DEFICIENT

Among other things, claim 1 further recites that the scalability port switch is to determine an address of one of said scaleable node controllers from said interrupt request. Tavallaei fails to teach or suggest this further recitation. In contrast to the present invention, Tavallaei describes a multi-processor system with local APICs 14 connected to the I/O APIC 26 over the APIC bus 16. Tavallaei describes that the I/O APIC 26 generates an interrupt message on the APIC bus 16, which is monitored by all the local APICs 14. The local APICs 14 appear to be responsive to the content of the interrupt messages for passing on local

interrupts for the associated processor 12. The Examiner has not identified (and applicants are unable to identify) any portion of Tavallaei that teaches or suggests that the local APICs 14 have addresses associated therewith.

The Examiner relies on a theory of inherency (at numbered paragraph 55) in order to read the Tavallaei reference on the claim recitations relating to an address for the scaleable node controller. However, the Examiner performs a clearly erroneous factual and legal analysis which fails to meet the burdens required by MPEP § 2112 for a rejection relying on inherency. The Examiner states "[o]ne of ordinary skill in the art would recognize that destination ID is a term that can be used for address." This is the incorrect legal test. Whether or not it 'can be used' is irrelevant to a legally correct theory of inherency. In order to be inherent, the Examiner must establish that it is the only possibility, not one of many that 'can be used.' This clear legal error by the Examiner requires reversal of the rejection.

Because Tavallaei fails to teach or suggest any of the recited scaleable node controller, scalability port switch, or an address for the scaleable node controller, claim 1 is not anticipated by Tavallaei, and is patentable over Tavallaei. Claims 2-3 depend from claim 1 and are likewise patentable.

Claims 9-10, 12, 16-19, 21 and 25-26

With respect to claims 9 and 18, for the reasons given above Tavallaei does not disclose the recited scaleable node controller or the recited scalability port switch when properly construed. Claims 9 and 18 further recite that determining the scaleable node controller includes determining an address of the scaleable node controller. For the reasons given above, the Examiner's reliance on inherency is legally deficient and Tavallaei does not disclose determining an address of the local APIC 14.

Accordingly, claim 9 and its dependent claims 10-12 and 16-17 are not anticipated by and are patentable over Tavallaei. Likewise, claim 18 and its dependent claims 19-21 and 25-26 are patentable over Tavallaei.

Claims 11 and 20

With respect to claims 11 and 20, the office action identifies col. 7 lines 41-44 of Tavallaei for the recited comparing a priority of the interrupt request with a priority of the processor. However, the cited portion makes no reference whatsoever to a priority of the processor. Accordingly, claims 11 and 20 are separately patentable over Tavallaei.

Applicants previously requested a complete and proper rejection meeting the requirements of MPEP § 2112 or withdrawal of the rejection. However, the Examiner has failed to comply. Applicants note that 'it is inherent' does not mean 'it is possible'. In any event, the rejection is based on clear legal error and should be reversed.

II. The rejection of claims 1-3, 9-12, 14-21, and 23-26 under 53 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,944,809 (Olarig) is in error and should be reversed.

Claims 1-3

In order to anticipate, the reference must identically disclose each claim element. In fact, Olarig does not identically disclose many of the recited claim elements when properly construed.

THE EXAMINER MISCONSTRUES THE CLAIM TERM 'SCALEABLE NODE CONTROLLER.'

The office action asserts that components 107 and 306 in Figure 4 of Olarig correspond to the recited scaleable node controllers. However, Olarig describes component 107 as a cache and component 306 as a local programmable interrupt controller (LOPIC). A cache and a LOPIC are not identical to a scaleable node controller.

As previously pointed out, the Examiner does not answer and apparently concedes applicants' argument that the different terminology in fact describes different structure and functionality. The Examiner does not answer and apparently concedes applicants' argument that a cache has no relationship whatsoever in structure or functionality to a node controller. The Examiner does not answer and apparently concedes applicants' argument that with respect to the LOPIC 306, every 'controller' does not perform the same function as every other 'controller'. The Examiner does not answer and apparently concedes applicants' argument that one skilled in the art would appreciate that a node controller performs a different function than an interrupt controller. The Examiner does not answer and apparently concedes applicants' argument that one skilled in the art would appreciate that a node controller has a different structure from an interrupt controller. The Examiner does not answer and apparently concedes applicants' argument that a node controller may have suitable structure to participate in an interrupt handling scheme, but an interrupt controller would not have suitable structure to perform the function of controlling a node of a multi-node system.

Applicants do not, as asserted by the Examiner, argue simply that because the terminology is different the reference does not read on the claims. The Examiner can refer back to the immediately preceding paragraph to review applicants' concrete, technical arguments as to why the different terminology actually refers to important differences in the technology.

Again, the question is not whether applicants' specification provides a discrete definition for each claim recitation. Applicants submit that providing such discrete definitions in a patent application is the exception, rather than the norm. When performing claim construction, the Examiner may consult the specification for such definitions, but in their absence the claim term must be construed as it would be understood by one of ordinary skill in the art as of the filing date of the application. Does the Examiner seriously contend that as of the filing date of the present application, a node controller would have no clear meaning to one of ordinary skill in the art?

The Examiner again commits clear legal error in his claim construction. As is set forth in MPEP § 2111.01(II), "[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, *i.e.*, as of the effective filing date of the patent application." Several examples set forth in MPEP § 2111.01(II) specifically state that where no definition is provided in the specification, the claim terms should be interpreted with the ordinary and customary meaning the terms would have to one skilled in the art. The Examiner has not even attempted to identify or set forth what the term 'scaleable node controller' would mean to a person of ordinary skill in the art at the time of the invention. This is clear legal error that requires reversal of the rejection.

The Examiner uses the fact that the specification does not provide a definition for these terms as an excuse to substitute his own, unreasonably broad definition of the terms. In the Examiner's view, any component that performs any control function in connection with any processing element reads on a scaleable node controller. Applicants submit that this may be the broadest possible interpretation, but it is not a reasonable interpretation and is also legally erroneous by failing to consider what the disputed terms would mean to one skilled in the art.

The Board can resolve this error by answering the following simple question. Namely, would one of ordinary skill in the art as of December 29, 2000, without any knowledge of applicants' own invention, have considered the cache 107 and LOPIC 306 described by Olarig to be a scaleable node controller? Applicants' submit that the answer to this question is no, and the rejection should be reversed.

THE EXAMINER MISCONSTRUES THE CLAIM TERM 'SCALABILITY PORT SWITCH.'

The office action asserts that component 312 in Figure 4 of Olarig corresponds to the recited scalability port switch. However, Olarig describes component 312 as a central

programmable interrupt controller (COPIC). A COPIC is not identical to a scalability port switch.

The Examiner does not answer and apparently concedes applicants' argument that the different terminology in fact describes different structure and functionality. The Examiner does not answer and apparently concedes applicants' argument that every controller does not perform the same function as every other controller. The Examiner does not answer and apparently concedes applicants' argument that one skilled in the art would appreciate that a port switch performs a different function than an interrupt controller. The Examiner does not answer and apparently concedes applicants' argument that one skilled in the art would appreciate that a port switch has a different structure from an interrupt controller. The Examiner does not answer and apparently concedes applicants' argument that a port switch may have suitable structure to participate in an interrupt handling scheme, but an interrupt controller would not have suitable structure to perform the function of switching ports of a multi-node system. The Examiner does not answer and apparently concedes applicants' argument that in some applications a port switch may include structure to resolve node addresses and that the COPIC 312 appears to lack such structure.

Applicant again notes that when performing claim construction, the Examiner may consult the specification for discrete definitions of claim terms, but in their absence the claim term must be construed as it would be understood by one of ordinary skill in the art as of the filing date of the application. Does the Examiner seriously contend that as of the filing date of the present application, a port switch would have no clear meaning to one of ordinary skill in the art?

The Examiner again commits clear legal error in his claim construction. As is set forth in MPEP § 2111.01(II), "[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, *i.e.*, as of the effective filing date of the patent application." Several examples set forth in MPEP § 2111.01(II) specifically state that where no definition is provided in the specification, the claim terms should be interpreted with the

ordinary and customary meaning the terms would have to one skilled in the art. The Examiner has not even attempted to identify or set forth what the terms 'scalability port switch' would mean to a person of ordinary skill in the art at the time of the invention. This is clear legal error that requires reversal of the rejection.

The Examiner uses the fact that the specification does not provide a definition for these terms as an excuse to substitute his own, unreasonably broad definition of the terms. In the Examiner's view any component that performs an I/O function reads on a scalability port switch. Applicants submit that this may be the broadest possible interpretation, but it is not a reasonable interpretation and is also legally erroneous by failing to consider what the disputed terms would mean to one skilled in the art.

The Board can resolve this error by answering the following simple question. Namely, would one of ordinary skill in the art as of December 29, 2000, without any knowledge of applicants' own invention, have considered the COPIC 312 described by Olarig to be a scalability port switch? Applicants' submit that the answer to this question is no, and the rejection should be reversed.

THE EXAMINER'S THEORY OF INHERENCY IS LEGALLY DEFICIENT

Among other things, claim 1 further recites that the scalability port switch is to determine an address of one of said scaleable node controllers from said interrupt request. Olarig fails to teach or suggest this further recitation. In contrast to the present invention, Olarig describes a multi-processor system with LOPICs 306 connected to the COPIC 312 over the PIC bus 311. Olarig appears to function similarly to Tavallaei as discussed above. The Examiner has not identified (and applicants are unable to identify) any portion of Olarig that teaches or suggests that the LOPICs 306 have addresses associated therewith.

In the Examiner's response to arguments, at numbered paragraph 58, the Examiner has now clarified that the rejection relies on a theory of inherency. As noted in MPEP §

2112, the fact that a feature may be present in the reference is not sufficient to establish inherency. The Examiner has the burden of proving that the LOPIC 306 must have an address associated therewith. However, this is burden cannot be met. Any of a number of schemes may be utilized for getting data to the appropriate processor 106. For example, the processor 106 in Olarig may include a processor ID and the message on the bus 311 may include the processor ID (e.g. similarly to Tavallaei as discussed above). Olarig expressly describes that the LOPIC maintains a register with the processor ID and the processor ID is used for delivering interrupts (see col. 7, lines 46-51). Because the data delivery scheme in Olarig might not use an address for the LOPIC 306, the reliance on inherency (and the rejection) fails.

The Examiner has not offered any technical explanation as to why the LOPIC 306 must necessarily include an address. Accordingly, the Examiner has not met the legal burden required to rely on a theory of inherency.

Because Olarig fails to teach or suggest any of the recited scaleable node controller, scalability port switch, or an address for the scaleable node controller, claim 1 is not anticipated by Olarig, and is patentable over Olarig. Claims 2-3 depend from claim 1 and are likewise patentable.

Claims 9-10, 12, 16-19, and 21-26

With respect to claims 9 and 18, for the reasons given above Olarig does not disclose the recited scaleable node controller, the recited scalability port switch, or the recited address of the scaleable node controller, when properly construed. Accordingly, claim 9 and its dependent claims 10-12 and 14-17 are not anticipated by and are patentable over Olarig. Likewise, claim 18 and its dependent claims 19-21 and 23-26 are patentable over Olarig.

Claims 11 and 20

With respect to claims 11 and 20, the office action identifies col. 10, lines 8-10 for the recited comparing a priority of the interrupt request with a priority of the processor. In the Examiner's response to arguments, in numbered paragraph 61, the Examiner further identifies col. 3, lines 4-7 for this recitation. Col. 3, lines 4-7 discusses only comparing the priority of the interrupt with priorities of other tasks. Col. 10, lines 8-10 (which has no connection with the other cited portion of col. 3, lines 4-7) discusses only comparing a processor task priority level with other processors to select the least busy processor. However, neither cited portion makes any reference whatsoever to comparing a priority of the interrupt request with a priority of the processor. Accordingly, claims 11 and 20 are separately patentable over Olarig.

In numbered paragraph 59, the Examiner relies on page 8, lines 16-17 of the present specification to improperly read limitations from the specification into the claims. The Examiner is respectfully directed to page 5, lines 25-27 of the present specification, which describes a priority of the processor.

III. The rejection of claims 4 and 5 under 35 U.S.C. § 103(a) as being unpatentable over Tavallaei in view of U.S. Patent No. 6,119,191 (Neal) is in error and should be reversed.

Neal fails to make up for the above-noted deficiencies in Tavallaei. Accordingly, the office fails to establish a prima facie case of obviousness.

Moreover, claim 4 recites a first input/output hub coupled between the peripheral component interconnect bus and the first scalability port switch, wherein said first input/output hub is able to support a plurality of additional peripheral component interconnect hubs. The office action asserts that component 28 corresponds to the recited hub. However, component 28 is simply described as an ASIC connected to a PCI bus, not an

I/O hub. In fact, the word "hub" cannot be found in Tavallaei. No one skilled in the art would be motivated to replace the ASIC 28 of Tavallaei with the hubs described in Neal.

In numbered paragraph 60, the Examiner yet again fails to give different terminology any relevance, even though the different terms in fact refer to different structures. One of ordinary skill in the art would appreciate that the ASIC 28 does not necessarily have the same structure or perform the same function as an I/O hub, just because it 'has inputs and outputs'.

Again, the question is not whether applicants' specification provides a discrete definition for each claim recitation. Applicants submit that providing such discrete definitions in a patent application is the exception, rather than the norm. When performing claim construction, the Examiner may consult the specification for such definitions, but in their absence the claim term must be construed as it would be understood by one of ordinary skill in the art as of the filing date of the application. Does the Examiner seriously contend that as of the filing date of the present application, an I/O hub would have no clear meaning to one of ordinary skill in the art?

The Examiner performs another clearly erroneous and overly broad claim construction. The Board should ask itself, would one of ordinary skill in the art as of December 29, 2000, without any knowledge of applicants' own invention, consider the ASIC 28 described by Neal to be an I/O hub? Applicants submit that the answer is clearly no, and that the claim construction set forth in the office action is a clearly erroneous attempt to stretch the reference beyond any reasonable reading in order to anticipate the claim.

Because the office action fails to establish a prima facie case of obviousness, and because the ASIC 28 is not an I/O hub, and because no one skilled in the art would be motivated to replace the ASIC 28 of Tavallaei with the hubs described in Neal, claim 4 is patentable over Tavallaei in view of Neal and the rejection should e reversed. Claim 5 depends from claim 4 and is likewise patentable.

IV. Claims 6 and 7 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Tavallaei, in view of Neal, and further in view of Intel's Multiprocessor Specification, dated May 1997 (MP).

Neal and MP both fail to make up for the above-noted deficiencies in Tavallaei. Accordingly, the office fails to establish a prima facie case of obviousness. Claim 6 and 7 depend from claim 5, and are accordingly patentable for the reasons given above. Claims 6 and 7 are further patentable for the following reasons.

Claim 6 recites that the first pair of scaleable node controllers and the second pair of scaleable node controllers are coupled to a second scalability port switch. Claim 7 depends from claim 6 and further recites that the second scalability port switch is coupled to the first input/output hub.

As noted in applicants' response filed August 18, 2006, the Examiner has not even attempted to read the references on several recitations of claim 6 and claim 7. Applicants note that the Examiner has no answer for this argument and apparently therefore concedes the allowability of these claims.

Because the office fails to establish a prima facie case of obviousness and because none of the cited references, individually or in combination, teach or suggest two pair of scaleable node controllers with each pair connected to two different scalability port switches, claims 6 and 7 are separately patentable over Tavallaei in view of Neal and further in view of MP.

V. The rejections of claims 13 and 22 under 35 U.S.C. § 103(a) as being unpatentable over either Tavallaei or Olarig in view of U.S. Patent No. 6,189,065 (Arndt) are in error and should be reversed.

For the Board's convenience, the claim language, the Examiner's stated rejection, and the cited portion of Arndt are reproduced below:

Claims 13 and 22	... wherein said scalable node controller redirects the interrupt request through the scalability port switch to a different processor.
Examiner's rejection	... Arndt discloses redirecting an interrupt to a different processor. Therefore it would have been obvious to combine the teachings of Arndt and [the primary reference] to redirect an interrupt to different processor since ...
Claim 8 Of Arndt	... an offload selector for offloading said interrupt message to a second processor if said first processor is busy servicing another interrupt signal ...

The claim language does not recite 'redirect an interrupt to a different processor'. The claim language recites that the scaleable node controller redirects the interrupt request through the scalability port switch to a different processor. The office action completely fails to address several of the claim recitations, and accordingly fails to establish a prima facie case of obviousness. The Examiner's response to arguments, in numbered paragraph 61, fails to clarify or explain the Examiner's position or answer applicants' previous traversal. In any event, the cited portion of Arndt is silent in regard to these claim recitations.

Because the Arndt fails to make up for the respective deficiencies in Tavallaei and Olarig, and because there is no motivation to combine the references as suggested by the office action, and because the Examiner fails to establish a prima facie case of obviousness, and because the cited portion of Arndt fails to describe that a scalable node controller redirects the interrupt request through a scalability port switch to a different processor, claims 13 and 22 are separately patentable over the cited combination of references.

CONCLUSION

In view of the foregoing, favorable reconsideration and reversal of the rejections is respectfully requested. Early notification of the same is earnestly solicited. If there are any questions regarding the present application, the Examiner and / or the Board is invited to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

November 20, 2006
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(viii) ***Claims appendix.***

1. An interrupt delivery system, comprising:

a first pair of scaleable node controllers, wherein each of said scaleable node controllers supports at least one microprocessor;

a first scalability port switch coupled to each of said scaleable node controllers, wherein said first scalability port switch is to receive an interrupt request, determine an address of one of said scaleable node controllers from said interrupt request and transmit said interrupt request to said one of said scaleable node controllers.

2. An interrupt delivery system as recited in claim 1, further comprising a peripheral component interconnect device.

3. An interrupt delivery system as recited in claim 2, further comprising a peripheral component interconnect bus coupled between the peripheral component interconnect device and the first scalability port switch, wherein said peripheral component interconnect bus is able to support a plurality of additional peripheral component interconnect devices.

4. An interrupt delivery system as recited in claim 3, further comprising a first input/output hub coupled between the peripheral component interconnect bus and the first scalability port switch, wherein said first input/output hub is able to support a plurality of additional peripheral component interconnect hubs.

5. An interrupt delivery system as recited in claim 4, further comprising a second pair of scaleable node controllers, wherein said second pair of scaleable node controllers are coupled to said first scalability port switch.

6. An interrupt delivery system as recited in claim 5, wherein the first pair of scaleable node controllers and the second pair of scaleable node controllers are coupled to a second scalability port switch.

7. An interrupt delivery system as recited in claim 6, wherein the second scalability port switch is coupled to the first input/output hub.

8. An interrupt delivery system as recited in claim 7, wherein the second scalability port switch is coupled to a second input/output hub, wherein said second input/output hub is able to support a plurality of additional peripheral component interconnect hubs and wherein each of the scaleable node controllers is coupled to four microprocessors.

9. A method for delivering an interrupt request in a multi-node computer system, comprising:

receiving an interrupt request at a scalability port switch;

determining an address of a scaleable node controller to receive said interrupt request; and

transmitting said interrupt request to said scaleable node controller.

10. A method for delivering an interrupt request in a multi-node computer system as recited in claim 9, further comprising determining a processor to receive the interrupt request.

11. A method for delivering an interrupt request in a multi-node computer system as recited in claim 10, further comprising comparing a priority of the interrupt request with a priority of the processor.

12. A method for delivering an interrupt request in a multi-node computer system as recited in claim 11, further comprising interrupting the processor.

13. A method for delivering an interrupt request in a multi-node computer system as recited in claim 11, wherein said scalable node controller redirects the interrupt request through the scalability port switch to a different processor.

14. A method for delivering an interrupt request in a multi-node computer system as recited in claim 9, wherein said interrupt request is a broadcast interrupt request.

15. A method for delivering an interrupt request in a multi-node computer system as recited in claim 12, further comprising transmitting an end of interrupt to a correct interrupt controller.

16. A method for delivering an interrupt request in a multi-node computer system as recited in claim 11, wherein the interrupt request is generated by a PCI device.

17. A method for delivering an interrupt request in a multi-node computer system as recited in claim 11, wherein the interrupt request is generated by a processor.

18. A set of instructions residing in a storage medium, said set of instructions capable of being executed by a processor for delivering an interrupt request in a multi-node computer system, the method comprising:

receiving an interrupt request at a scalability port switch;

determining an address of a scaleable node controller to receive said interrupt request; and

transmitting said interrupt request to said scaleable node controller.

19. A method for delivering an interrupt request in a multi-node computer system as recited in claim 18, further comprising determining a processor to receive the interrupt request.

20. A method for delivering an interrupt request in a multi-node computer system as recited in claim 19, further comprising comparing a priority of the interrupt request with a priority of the processor.

21. A method for delivering an interrupt request in a multi-node computer system as recited in claim 20, further comprising interrupting the processor.

22. A method for delivering an interrupt request in a multi-node computer system as recited in claim 20, wherein said scalable node controller redirects the interrupt request through the scalability port switch to a different processor.

23. A method for delivering an interrupt request in a multi-node computer system as recited in claim 18, wherein said interrupt request is a broadcast interrupt request.

24. A method for delivering an interrupt request in a multi-node computer system as recited in claim 21, further comprising transmitting an end of interrupt to a correct interrupt controller.

25. A method for delivering an interrupt request in a multi-node computer system as recited in claim 20, wherein the interrupt request is generated by a PCI device.

26. A method for delivering an interrupt request in a multi-node computer system as recited in claim 20, wherein the interrupt request is generated by a processor.

(ix) ***Evidence appendix.***

None.

(x) ***Related proceedings appendix.***

None.